HARDWARE DEVELOPMENT OF A CONTROL SYSTEM FOR A STEPPER MOTOR

1. Goals of the laboratory sessions

The goal of these laboratory sessions will consist in the design of the hardware controller that will permit to manage the two actuators included in the application to be solved. These actuators are stepper motors. The voltages applied to the motor windings are provided by the L6220 driver (one for each motor) from ST Microelectronics. Therefore, the final goal will consist in the design of a hardware controller able to generate the signals for every motor driver so that the motors can move one step in a given direction.

2. Introduction

In the case of the motors that will be used as actuators for the proposed application one step represents an angular movement of 1,8 º. The signals to be generated for the L6220 driver so as to produce the correct voltages on the motor windings in order to permit the motor to advance one step in a given direction are those depicted in figures 1 and 2.

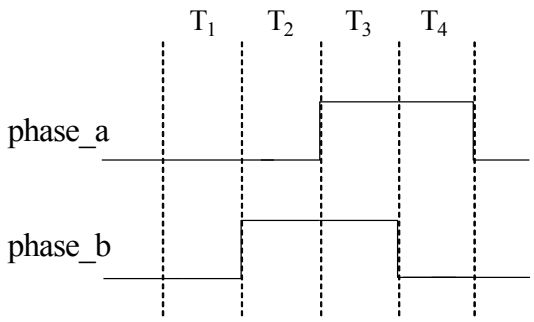

Figure 1.

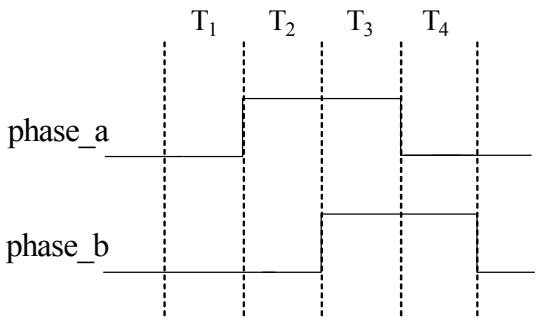

Figure 2.

When the signals phase_a and phase_b follow the sequence depicted in figure 1 the L6220 driver will apply to the motor windings voltages that will modify its angular position to the left for the motor whose axis is in vertical position or downwards for the motor whose axis is in horizontal position. When the signals phase_a and phase_b follow the sequence depicted in figure 2 the L6220 driver will apply to the motor windings voltages that will modify its angular position to the right for the motor whose axis is in vertical position or upwards for the motor whose axis is in horizontal position. The combination of signals phase_a and phase_b in each interval T_1, T_2, T_3 and T_4 will produce an angular displacement of the motor of 1,8º. The duration of these intervals will be 1 ms. In order to avoid undesirable transient movements in the motors the signals phase_a and phase_b have to be registered.

3. Specification of the development

The development of the system will be divided in two parts. The first part will be devoted to the development of the controller for a single motor. In the second part it will be necessary to design a system able to process the commands that permit to move the camera one step up (54), to the right (55), to the left (56) or down (57).

The first system to be designed will have four inputs, called ***enable***, ***direction***, ***clearn*** and ***clk*** and three outputs, called ***phase_a***, ***phase_b*** and ***movement***. The meaning of these signals is the following:

- **clk:** Clock signal of the system. Its frequency is 50 MHz, and it will be act on the memory elements on its rising edge.
- **clearn:** Synchronous reset of the system. Active low.
- **direction:** Indicates the direction of the movement of the motor. A value '0' implies a movement to the left or downwards, while a value '1' implies a movement to the right or downwards.
- **enable:** Enable signal. Its duration is one period of the clock signal ***clk***. It will permit the motor to move one step as indicated by the ***direction*** input.
- **phase_a:** First phase output for the motor driver.
- **phase_b:** Second phase output for the motor driver.
- **movement:** This signal indicates if the motor is moving (level '1') as indicated by the controller or not (level '0').

The second system to be designed will have five inputs, called ***PCS0n***, ***RDn***, ***command***, ***clk*** and ***clearn*** and six outputs, called ***phase_a_vertical***, ***phase_b_vertical***, ***phase_a_horizontal***, ***phase_b_horizontal***, ***movement_vertical*** and ***movement_horizontal***. The meaning of these signals is the following:

- **PCS0n:** Chip select 0 signal of the SC12 device. Active low. When this signal is active the SC12 device is carrying out a transfer on the input/output space whose base address is indicated by this signal.
- **RDn:** Read signal of the SC12 device. Active low. Indicates that the SC12 device is performing a read access on its AD bus.
- **command:** This signal, 6-bit wide, will contain the 6 least significant bits of the AD bus of the SC12 device. This value has to be registered using as enable signals the inputs ***PCS0n*** and ***RDn***.
- **clk:** Clock signal of the system. Its frequency is 50 MHz, and it will be act on the memory elements on its rising edge.
- **clearn:** Synchronous reset of the system. Active low.
- **phase_a_vertical:** First phase signal for the driver that controls the motor whose axis is in vertical position.
- **phase_b_vertical:** Second phase signal for the driver that controls the motor whose axis is in vertical position.
- **phase_a_horizontal:** First phase signal for the driver that controls the motor whose axis is in horizontal position.
- **phase_b_horizontal:** Second phase signal for the driver that controls the motor whose axis is in horizontal position.
- **movement_vertical:** This signal indicates that the motor whose axis is in vertical position is moving.

- **movement_horizontal:** This signal indicates that the motor whose axis is in horizontal position is moving.

The second system will be used as a component within an entity in a higher hierarchy level whose VHDL description will be provided in the laboratory. This entity, together with a configuration file, Hill permit to verify the design on a Xilinx XCS200E-PQ208 programmable device included in the D2-SB development board. To facilitate the instantiation of the component designed the name of its entity should be ***control_motors***. It is also recommended to keep the name and the order for the signals that constitute its input/output interface as indicated previously. Otherwise it will be necessary to modify the VHDL file provided in the laboratory.

In order to debug the design the DIO input/output board will be used. In this board it will be possible to set values for the inputs ***PCS0n***, ***RDn***, ***command*** and ***clearn*** using switches. The six output signals of the system to be designed will be visualised using a logic analyser. The information regarding the proper setting for the board switches and the location of the points to be analysed will be provided in the laboratory.