

## QUAD DARLINGTON SWITCHES

### 1 FEATURES

- FOUR NON INVERTING INPUTS WITH ENABLE
- OUTPUT VOLTAGE UP TO 50V
- OUTPUT CURRENT UP TO 1.8A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

### 2 DESCRIPTION

The L6220 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common inhibit input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darling-

Figure 1. Package

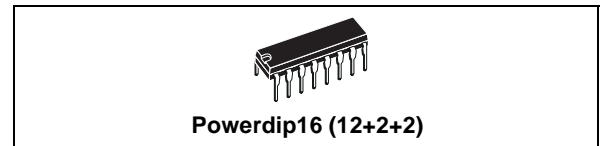


Table 1. Order Codes

Part Number	Package
L6220	Powerdip16

ton transistor plus a fast diode for switching applications with inductive loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

The L6220 is mounted in a Powerdip 12 + 2 + 2 package.

Figure 2. Block Diagram

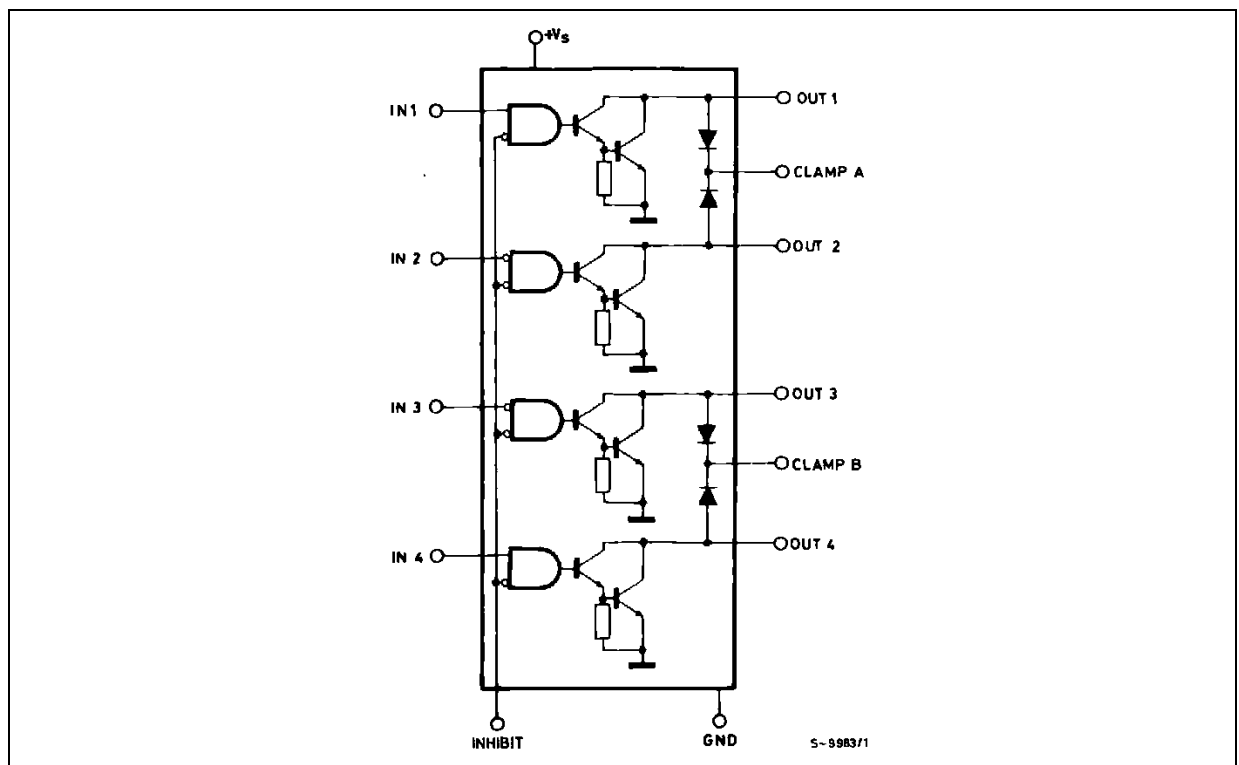


Table 2. Pin Description

Pin N#	Pin Name	Function
1	OUT 4	Output of Driver 4
2	CLAMP B	Diode Clamp to Driver 3 and Driver 4
3	OUT 3	Output of Driver 3
4, 5, 12, 13	GND	Common Ground
6	OUT 2	Output of Driver 2
7	CLAMP A	Diode Clamp to Driver 1 and Driver 2
8	OUT 1	Output of Driver 1
9	IN 1	Input to Driver 1
10	IN 2	Input to Driver 2
11	V <sub>S</sub>	Logic Supply Voltage
14	INHIBIT	Inhibit Input to all Drivers
15	IN 3	Input to Driver 3
16	IN 4	Input to Driver 4

Figure 3. Pin Connections

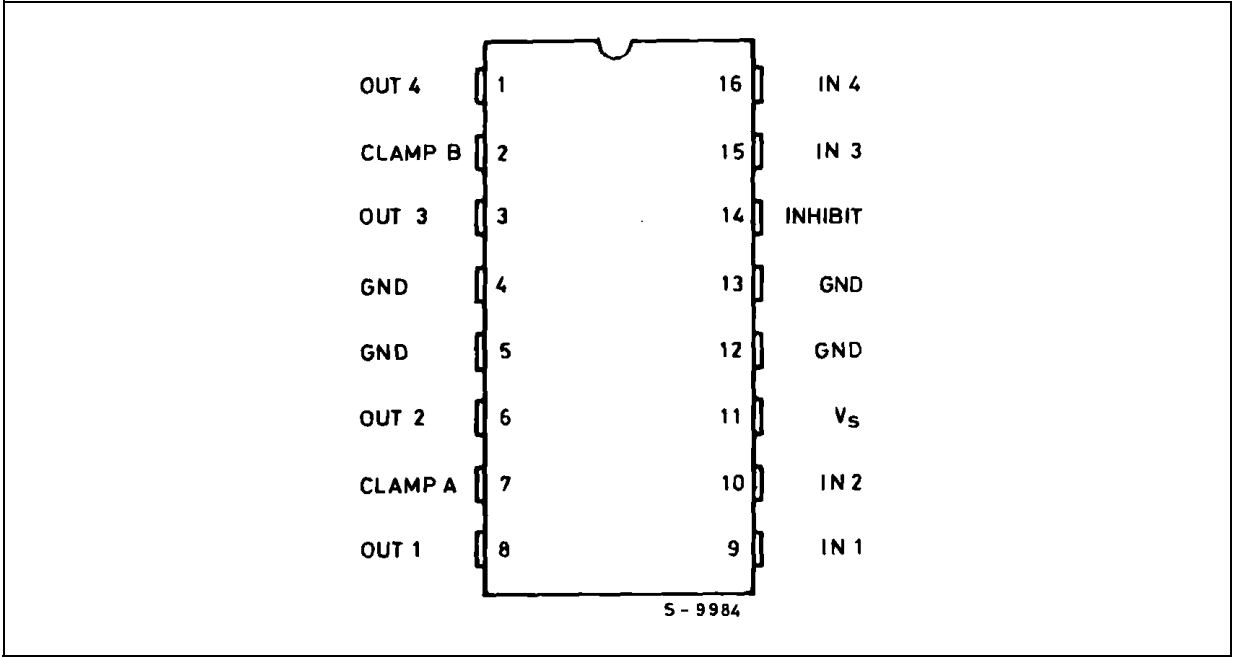


Table 3. TRUTH TABLE

Enable	Inputs 1, 4	Power Out	Enable	Inputs 2, 3	Power Out
L	H	ON	L	L	ON
L	L	OFF	L	H	OFF
H	X	OFF	H	X	OFF

For each input : H = High level  
L = Low level

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$V_o$	Output Voltage	50	V
$V_s$	Logic Supply Voltage	7	V
$V_{IN}, V_{EN}$	Input Voltage, Enable Voltage	$V_s$	
$I_C$	Continuous Collector Current (for each channel)	1.8	A
$I_C$	Collector Peak Current (repetitive, duty cycle = 10 % $t_{on} = 5$ ms)	2.5	A
$I_C$	Collector Peak Current (non repetitive, $t = 10$ $\mu$ s)	3.2	A
$T_{op}$	Operating Temperature Range (junction)	- 40 to + 150	°C
$T_{stg}$	Storage Temperature Range	- 55 to + 150	°C
$I_{sub}$	Output Substrate Current	350	mA
$P_{tot}$	Total Power Dissipation at $T_{pins} = 90$ °C at $T_{amb} = 70$ °C	4.3 1	W W

Table 5. Thermal Data

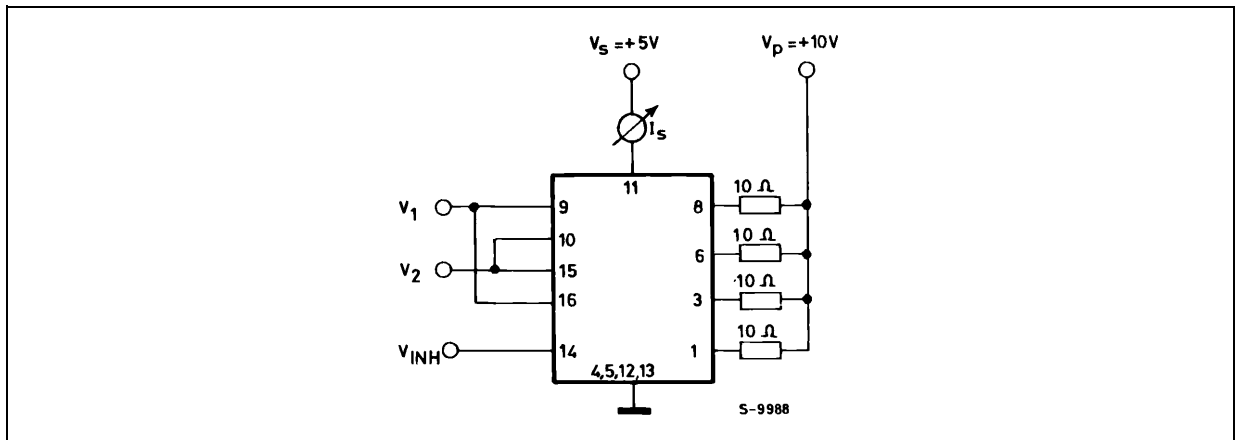
Symbol	Parameter	Value	Unit
$R_{th\ j-pins}$	Thermal Resistance Junction-pins Max.	14	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient Max.	80	°C/W

Table 6. Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_s$	Logic Supply Voltage		4.5		5.5	V
$I_s$	Logic Supply Current	All Outputs ON, $I_C = 0.7$ A			20	mA
		All Outputs OFF			20	mA
$V_{CE(sus)}$	Output Sustaining Voltage	$I_C = 100$ mA, $V_{IN} = V_{INH}$	46			V
$I_{CEX}$	Output Leakage Current	$V_{CE} = 50$ V, $V_{IN\ 1.4} = V_{INH}$			1	mA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage (one input on ; all others inputs off.)	$V_s = 4.5$ V $V_{IN\ 2.3} = V_{INL}$ , $V_{INH} = V_{INH\ L}$ $I_C = 0.6$ A $I_C = 1$ A $I_C = 1.8$ A			1 1.2 1.6	V
$V_{INL}$ , $V_{INH\ L}$	Input Low Voltage				0.8	V
$I_{INL}$ , $I_{INH\ L}$	Input Low Current	$V_{IN} = V_{INL}$ , $V_{EN} = V_{ENL}$			- 100	$\mu$ A
$V_{INH}$ , $V_{INH\ H}$	Input High Voltage		2.0			V
$I_{INH}$ , $I_{INH\ H}$	Input High Current	$V_{IN} = V_{INH}$ , $V_{INH} = V_{INH\ H}$			$\pm 10$	$\mu$ A
$I_R$	Clamp Diode Leakage Current	$V_R = 50$ V, $V_{INH} = V_{INH\ H}$			100	$\mu$ A
$V_F$	Clamp Diode Forward Voltage	$I_F = 1$ A			1.6	V
		$I_F = 1.8$ A			2.0	V
$t_d\ (on)$	Turn on Delay Time	$V_p = 5$ V, $R_L = 10\Omega$			2	$\mu$ s
$t_d\ (off)$	Turn off Delay Time	$V_p = 5$ V, $R_L = 10\Omega$			5	$\mu$ s
$\Delta I_s$	Logic Supply Current Variation	$V_{IN} = 5$ V, $V_{EN} = 5$ V $I_{out} = - 300$ mA for Each Channel			120	mA

### 3 TEST CIRCUITS

Figure 4. Logic supply current.



Set  $V_1 = 4.5\text{V}$ ,  $V_2 = 0.8\text{V}$ ,  $V_{INH} = 4.5\text{V}$  or  $V_1 = 0.8\text{V}$ ,  $V_2 = 4.5\text{V}$ ,  $V_{INH} = 0.8\text{V}$  for  $I_S$  (all outputs off)  
 Set  $V_1 = 2\text{V}$ ,  $V_2 = 0.8\text{V}$ ,  $V_{INH} = 0.8\text{V}$  for  $I_S$  (all outputs on)

Figure 5. Output Sustaining Voltage.

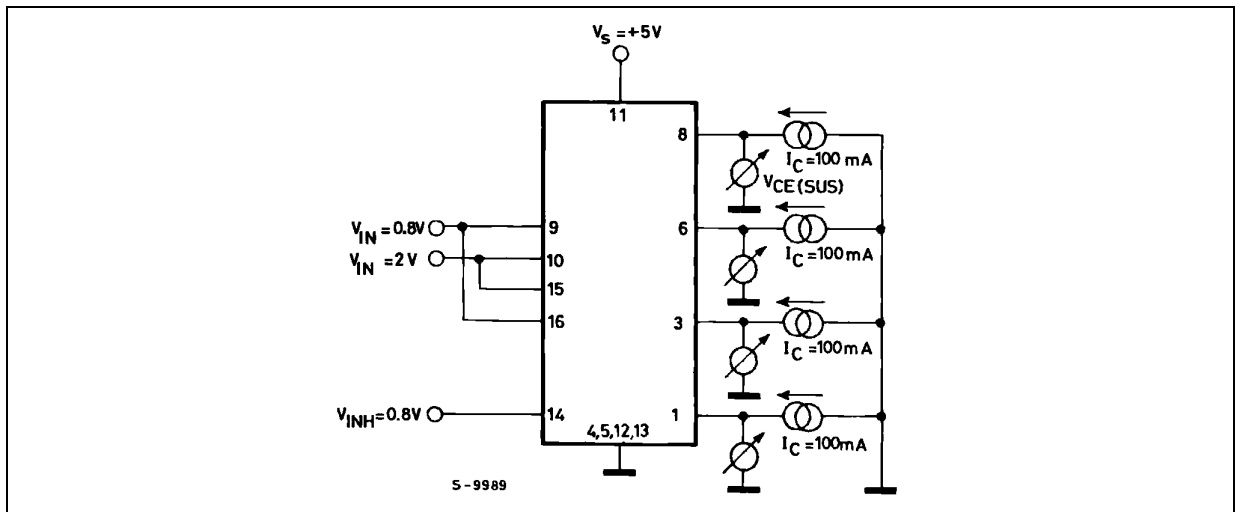


Figure 6. Output Leakage Current.

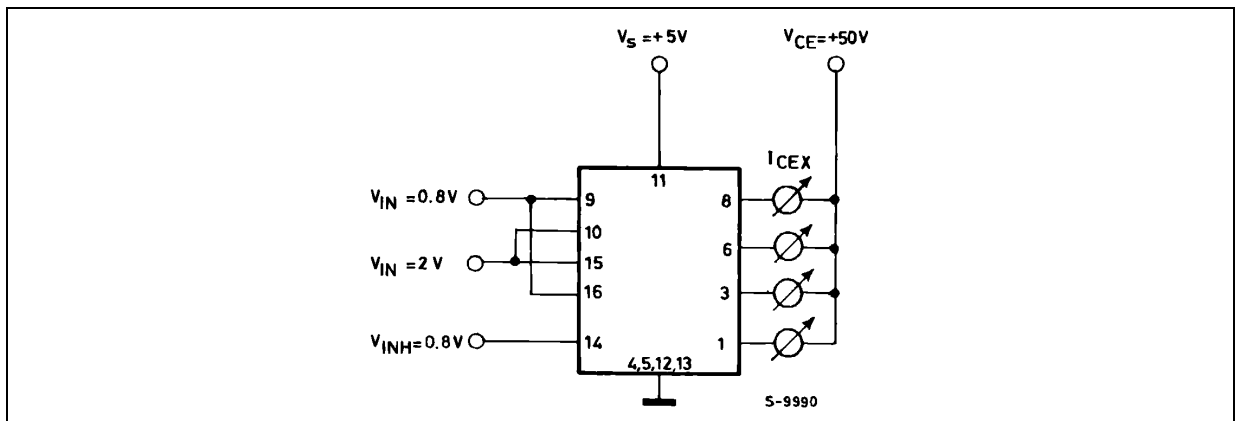


Figure 7. Collector-emitter Saturation Voltage

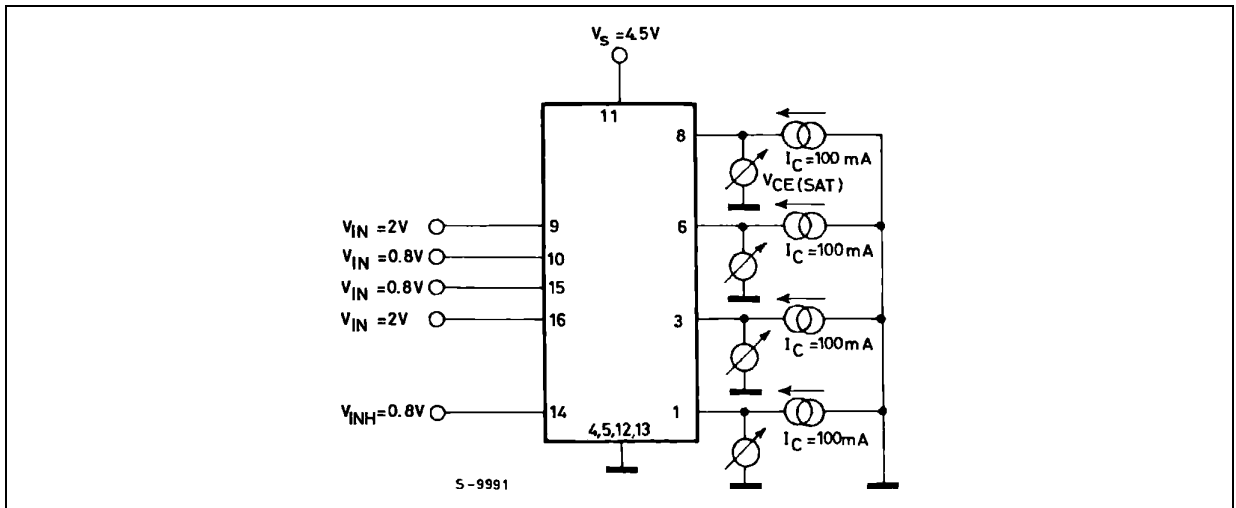
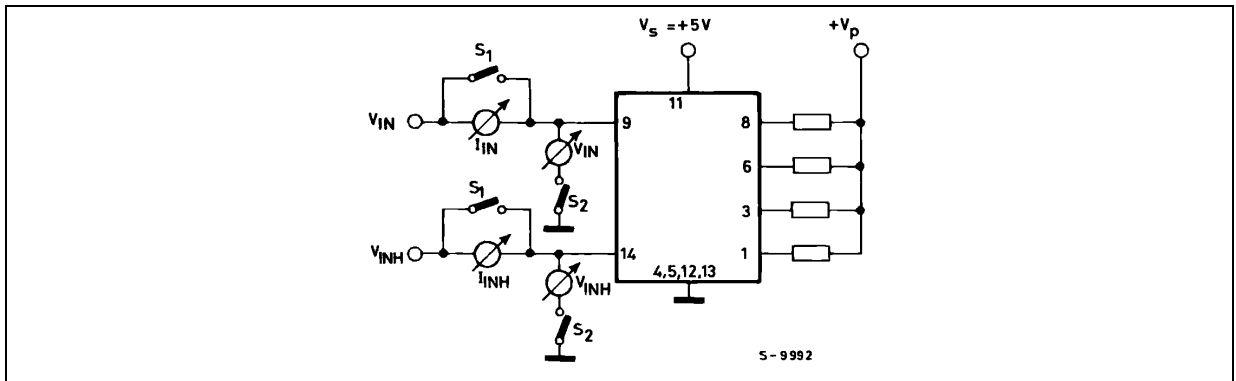


Figure 8. Logic Input Characteristics



Set  $S_1, S_2$  open,  $V_{IN}, V_{INH} = 0.8V$  for  $I_{IN} L, I_{INH} L$   
 Set  $S_1, S_2$  open,  $V_{IN}, V_{INH} = 2V$  for  $I_{IN} H, I_{INH} H$   
 Set  $S_1, S_2$  close,  $V_{IN}, V_{INH} = 0.8V$  for  $V_{IN} L, V_{INH} L$   
 Set  $S_1, S_2$  close,  $V_{IN}, V_{INH} = 2V$  for  $V_{IN} H, V_{INH} H$

Figure 9. Clamp Diode Leakage Current.

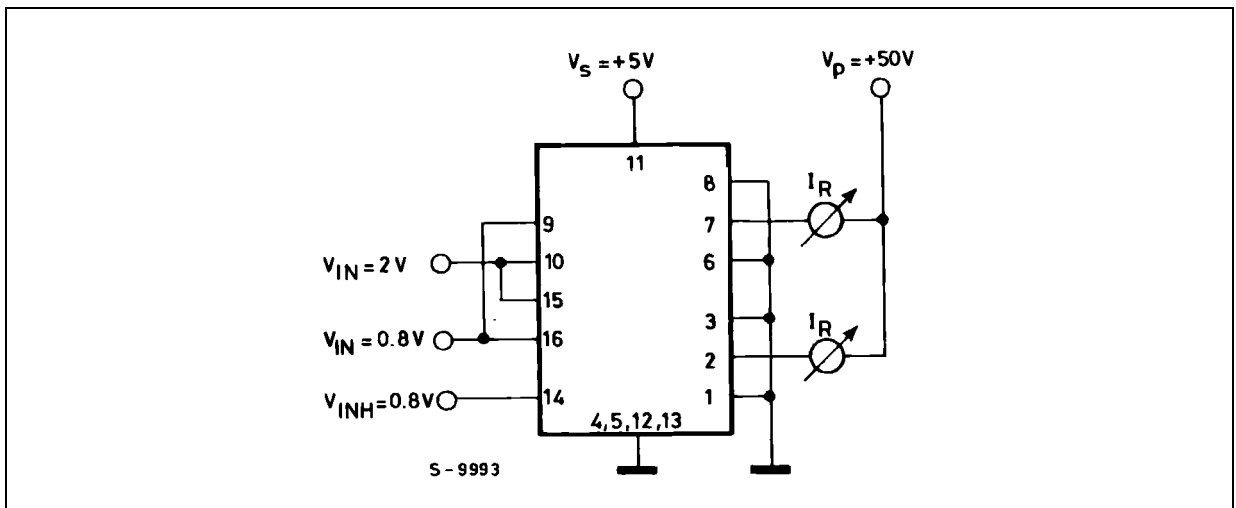


Figure 10. Clamp Diode Forward Voltage.

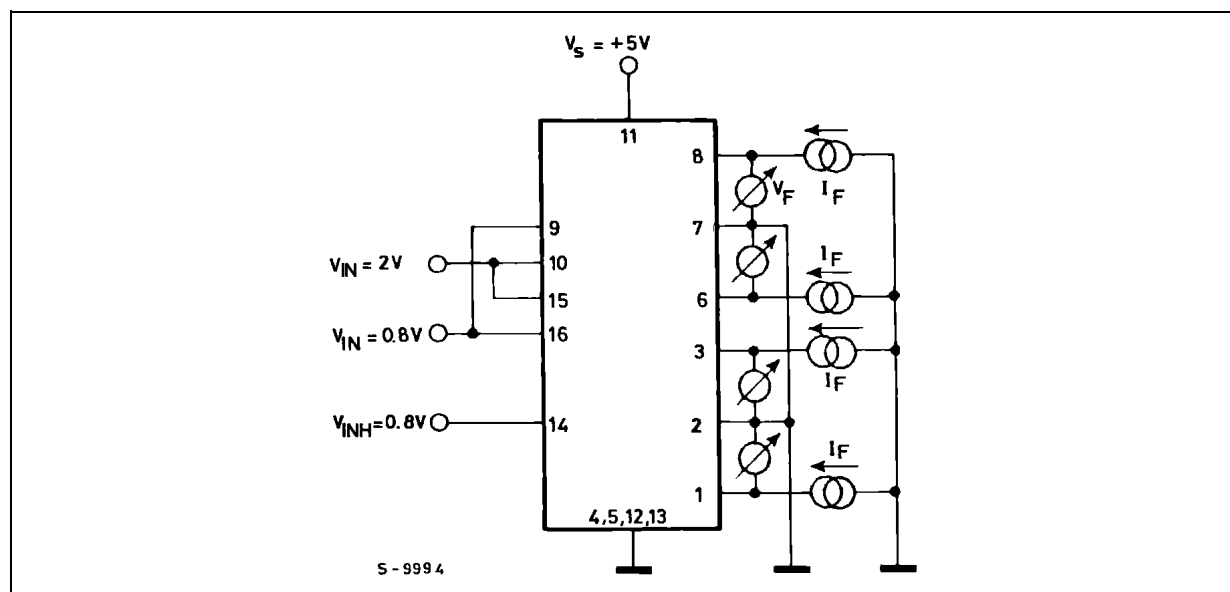


Figure 11. Switching Times Test Circuit.

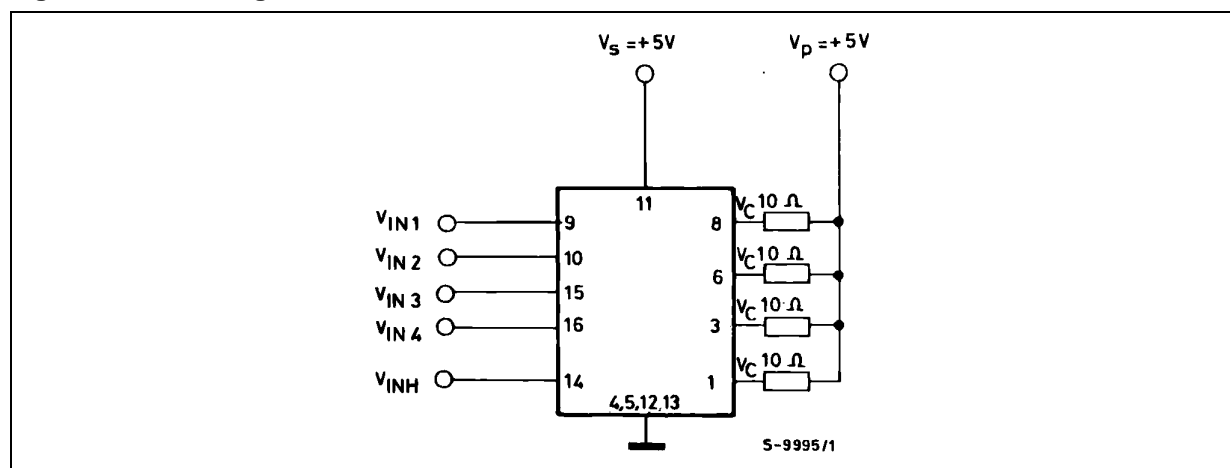
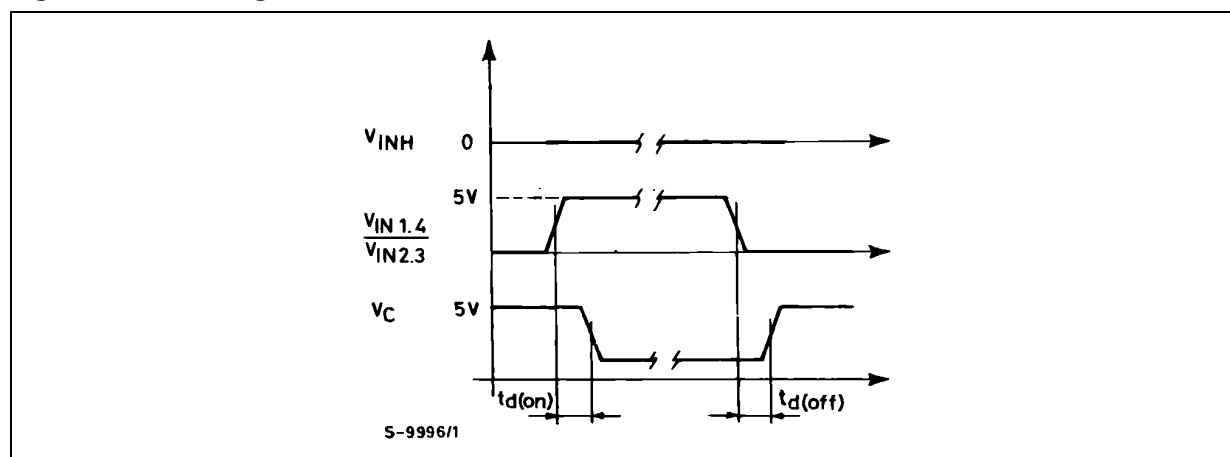
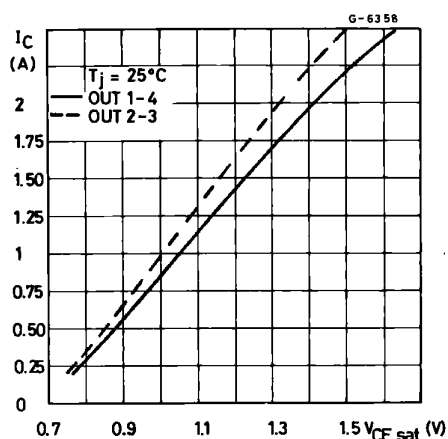


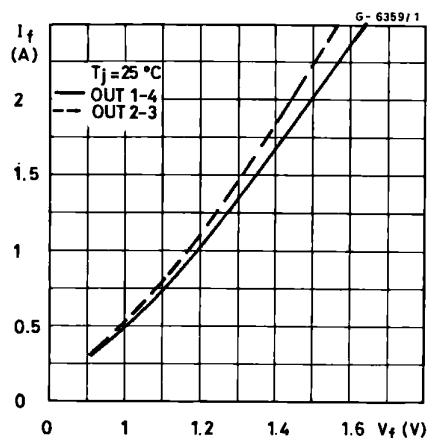
Figure 12. Switching Times Waveforms.



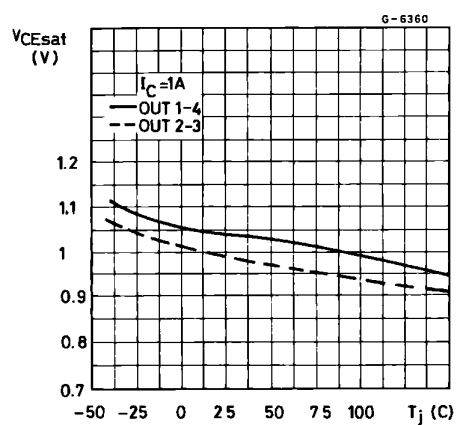
**Figure 13. Collector Saturation Voltage versus Collector Current**



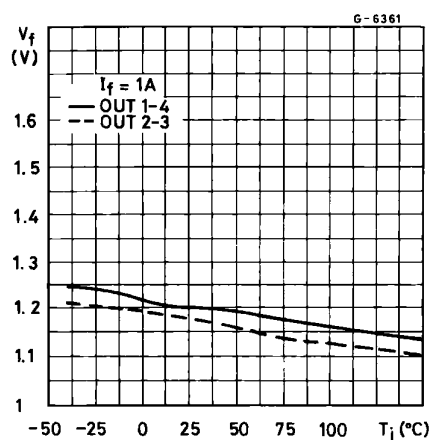
**Figure 14. Free-wheeling Diode Forward Voltage versus Diode Current**



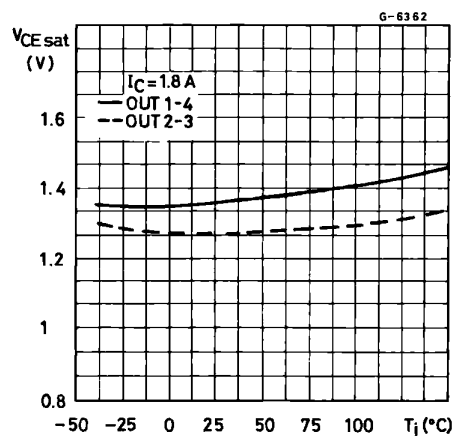
**Figure 15. Collector Saturation Voltage versus Junction Temperature at  $I_C = 1A$**



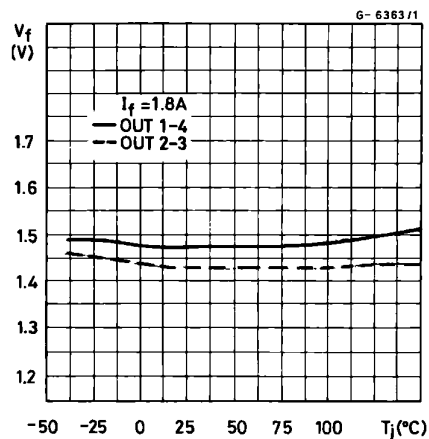
**Figure 16. Free-wheeling Diode Forward Voltage versus Junction Temperature at  $I_f = 1A$**



**Figure 17. Collector Saturation Voltage versus Junction Temperature at  $I_C = 8A$**



**Figure 18. Free-wheeling Diode Forward Voltage versus Junction Temperature at  $I_f = 1A$**



## 4 APPLICATION INFORMATION

When inductive loads are driven by L6220, a zener diode in series with the integral free-wheeling diodes increases the voltage across which energy stored in the load is discharged and therefore speeds the current decay (fig. 19).

Figure 19.

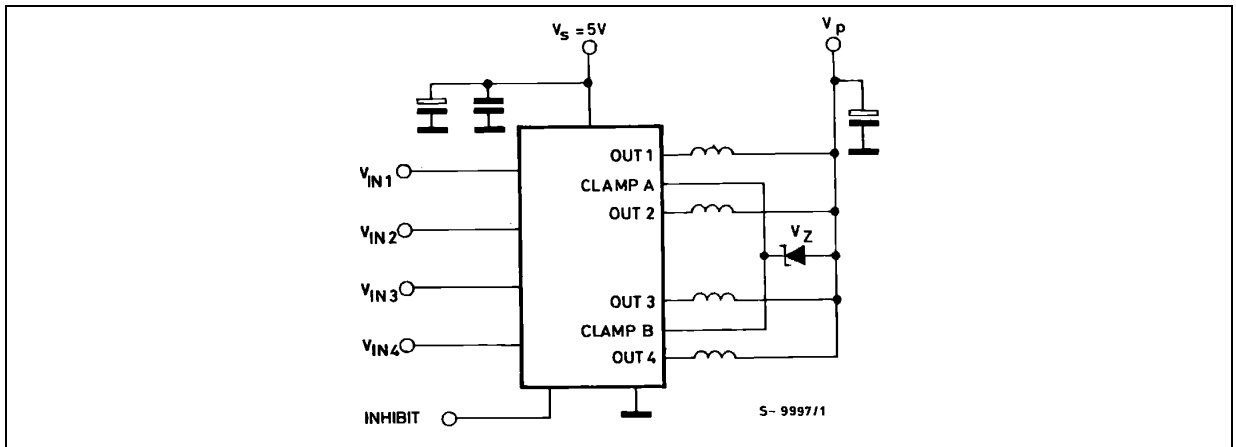
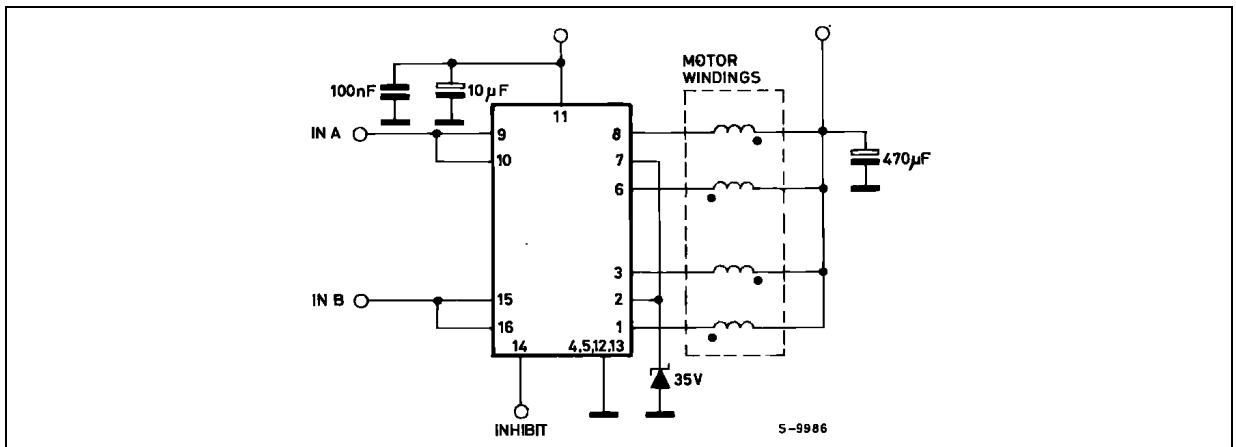


Figure 20. Unipolar Stepper Motor Driver.

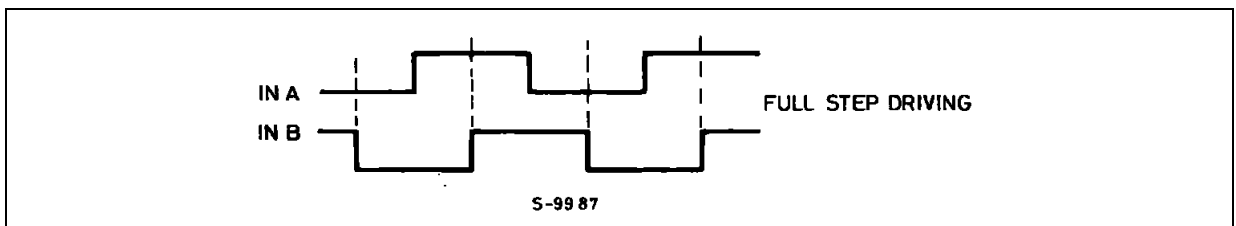


For reliability it is suggested that the zener is chosen so that  $V_P + V_Z < 35 V$ .

The reasons for this are two fold :

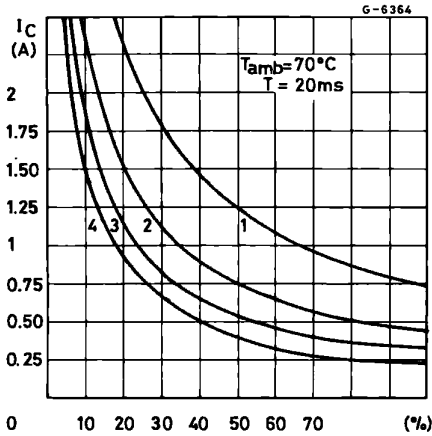
- 1) The zener voltage changes in temperature and current.
  - 2) The instantaneous power must be limited to avoid the reverse second breakdown.
- The particular internal logic allows an easier full step driving using only two input signals.

Figure 21.





**Figure 22. Allowed Peak Collector-current versus Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6220).**



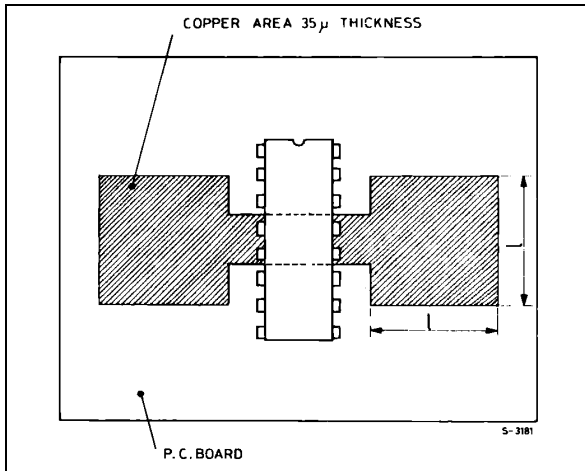
## 5 MOUNTING INSTRUCTION

The  $R_{th j-amb}$  of the L6220 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 24) or to an external heatsink (Fig. 25).

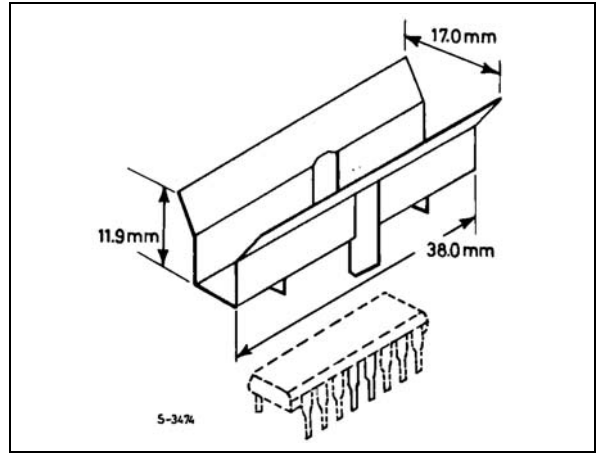
The diagram of figure 25 shows the maximum dissippable power  $P_{tot}$  and the  $R_{th j-amb}$  as a function of the side "a" of two equal square copper areas having a thickness of  $35\mu$  (1.4 mils). During soldering the pins temperature must not exceed  $260^\circ\text{C}$  and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

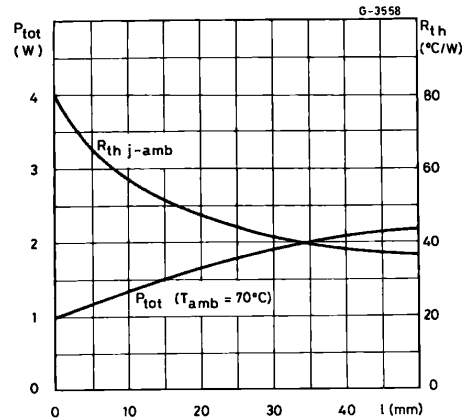
**Figure 23. Example of P.C. Board Copperarea which is used as Heatsink**



**Figure 24. External Heatsink Mounting Example**



**Figure 25. Maximum Dissippable Power and Junction to Ambient Thermal Resistance versus Side "a"**



**Figure 26. Maximum Allowable Power Dissipation versus Ambient Temperature**

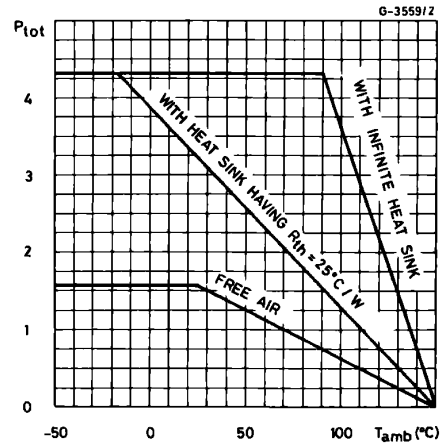
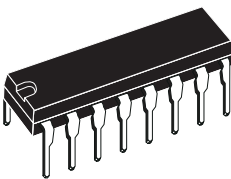


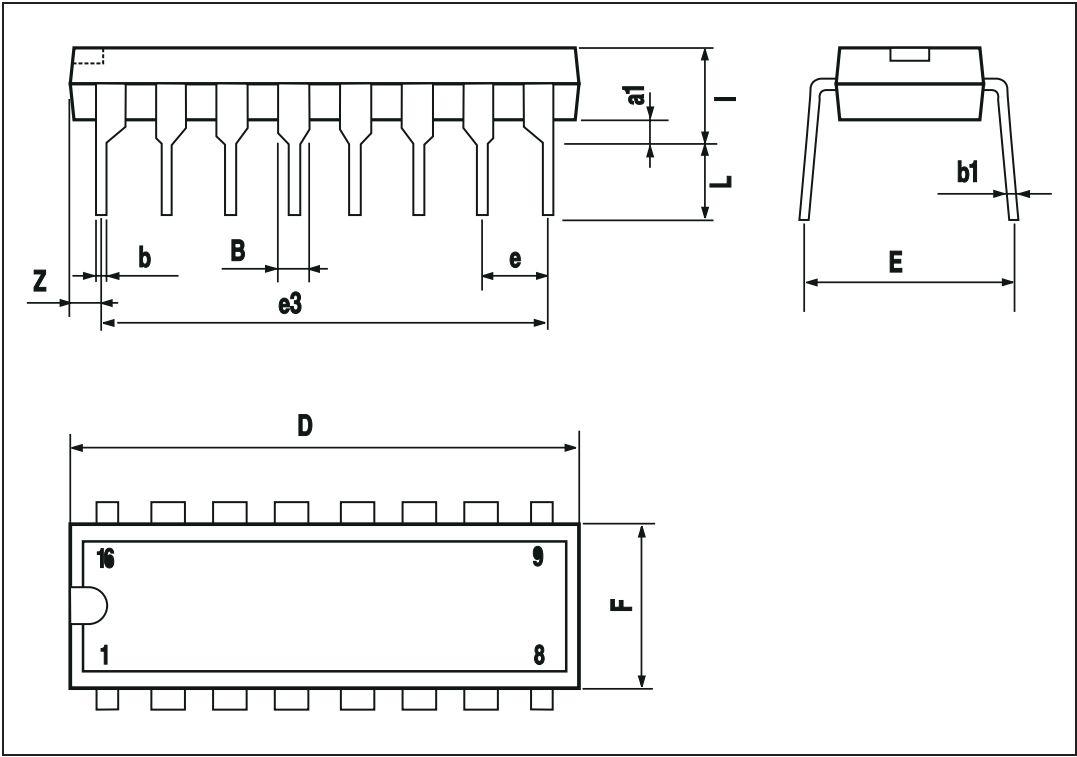
Figure 27. DIP16 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



DIP16



**Table 7. Revision History**

Date	Revision	Description of Changes
September 2003	1	First Issue
July 2004	2	Cancelled the L6220N part number and the relative references. Changed the style-look following the new "Corporate Technical Publications Design Guide" rules.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.  
All other names are the property of their respective owners

© 2004 STMicroelectronics - All rights reserved

**STMicroelectronics GROUP OF COMPANIES**

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -  
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States  
**[www.st.com](http://www.st.com)**